VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (three times amended) An integrated circuit package comprising:

a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings [and first and second surfaces], wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed;

a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer;

a chip adhered to said bottom [second] surface of said bottom layer of said substrate;

a plurality of electrical conductors physically attached to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate;

a plurality of pads disposed on said top [first] surface of said top layer of said substrate generally centralized within said peripheral openings of said substrate; and

potting material filling said peripheral openings.

2. (cancelled)

3. (amended) The integrated circuit package as recited in claim 1 wherein at least one of said pads disposed on said top surface of said top layer of said

substrate is electrically connected with said at least one of said routing strips [further comprising a plurality of routing strips being integral with said substrate].

4. (amended) The integrated circuit package as recited in claim 3 wherein at least one of said pads disposed on said top [first] surface of said top layer of said substrate is electrically connected with said at least one of said routing strips with a via through said top layer of said substrate.

8. (twice amended) An integrated circuit package comprising:

a multilayer substrate comprising a top layer having a top surface and a bottom layer having a bottom surface opposite said top surface, said top and said bottom layers having a plurality of overlapping peripheral openings, wherein said openings are larger in said top layer than in said bottom layer such that a portion of a top surface of said bottom layer is exposed; [having a plurality of peripheral openings and first and second surfaces];

a plurality of routing strips on said top surface of said bottom layer, wherein at least one of said routing strips is on said exposed portion of said top surface of said bottom layer [being integral with said substrate];

a plurality of pads disposed centrally on said top [first] surface, at least one of said pads being electrically connected with said at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate; and

wire bonding electrically connecting said chip to said substrate between at least one of said bonding pads and said at least one of said routing strips on said exposed portion of said top surface of said bottom layer.

15. (amended) The integrated circuit package as recited in claim 8 wherein said at least one of said pads being electrically connected with said at least one of said routing strips is connected by a via through said top layer of said substrate [6 wherein said substrate has first, second and third layers and wherein said first layer has a thickness of about 12 mils, said second layer has a thickness of about 8 mils and said third layer has a thickness of about 8 mils].

20. (amended) The integrated circuit package as recited in claim 19, wherein said peripheral openings in said second layer are larger than the peripheral openings in said first layer, such that a portion of a top surface of said first layer is exposed in each of said peripheral openings in said second layer [16 wherein said substrate has first, second and third layers and wherein said first layer has a thickness of about 12 mils, said second layer has a thickness of about 8 mils and said third layer has a thickness of about 8 mils].

22. (amended) An integrated circuit package comprising:

a substrate having a plurality of peripheral openings [opening] and first and second surfaces;

a chip comprising an operative side and a non-operative side, wherein said chip is adhered to said second surface of said substrate such that the non-operative side faces away from the substrate;

a plurality of pads disposed on said first surface of said substrate [generally centralized] within said peripheral openings of said substrate, said substrate having a substantially similar size to that of said chip such that no pads of said plurality of pads may be located on said substrate between said peripheral openings and an outside edge of said substrate; and

potting material filling said peripheral openings.